深圳市三元晶科技有限公司
ShenZhen TCC LCD Hi-Tech Co., Ltd.

液晶显示模组规格承认书
SPECIFICATION FOR LCM MODULE

客户名称(Customer Name)：	
客户料号(Customer P/N.)：	
模组型号(TCC P/N.)：	SY0128640960AV10-3C135WN2-WC
物料编号(TCC C/N.)：	
文件号(Version No.)：	A
日期(Date)：	2020-04-16

公司签核 (Signature)	管理者 (Manager)	市场 (Sales)	工程 (Engineering)	品保 (QA)
	LSS	WM	LXX	LW

客户确认 (Customer approval)	

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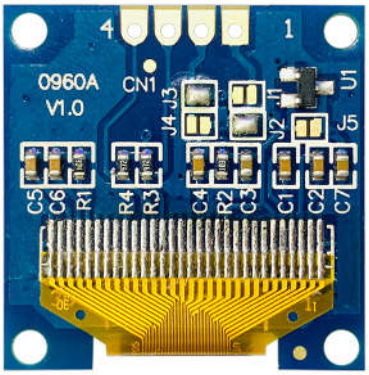
Dot matrix OLED display module Manual

SY0128640960AV10-3C135WN2-WC



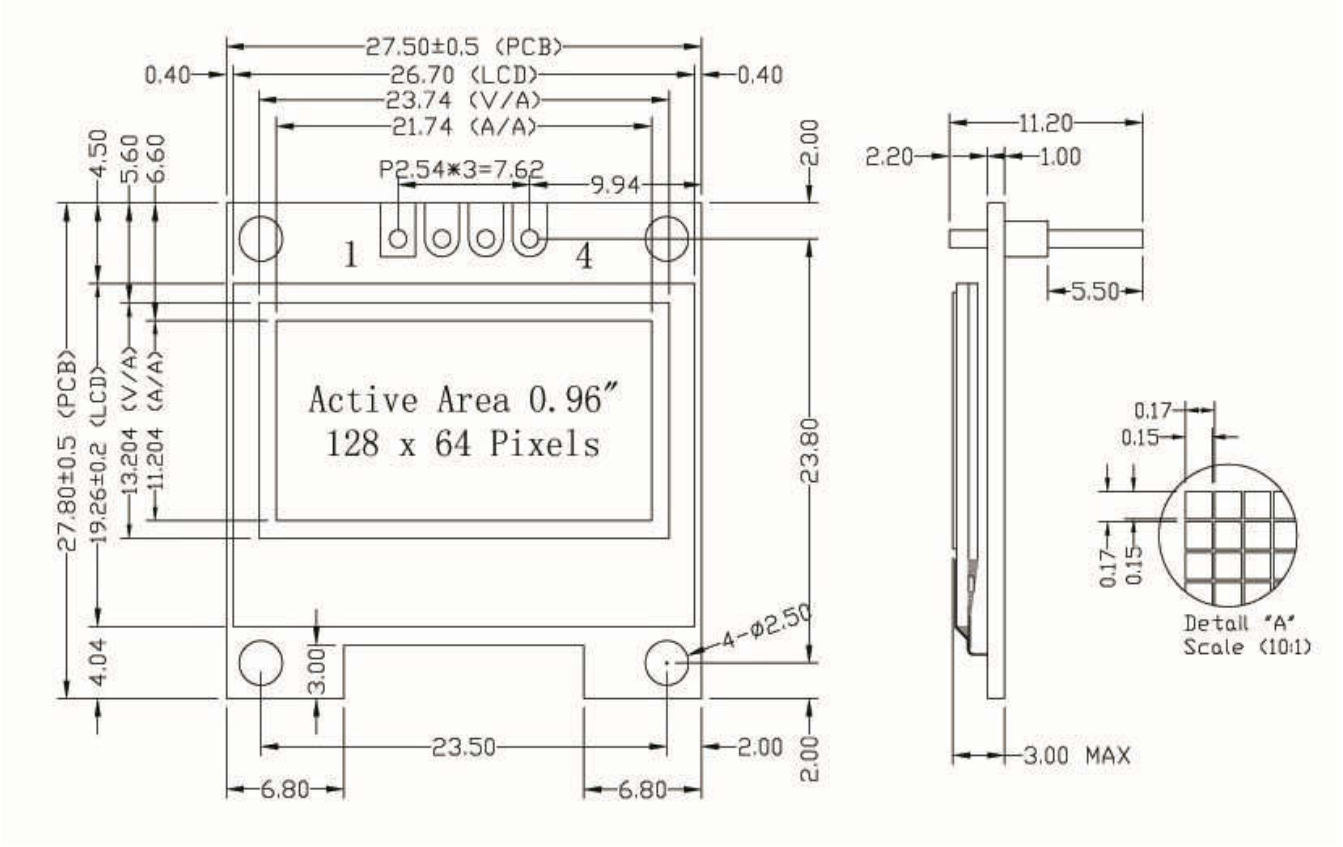
1. FUNCTIONS & FEATURES

- Display Mode: Passive Matrix
- Number of Pixels: 128×64 dots
- Display Color: Monochrome (White/Bule/Yellow-bule)
- Drive Duty: 1/64 Duty
- Driver IC: SSD1306 or SH1106
- Interface: IIC port

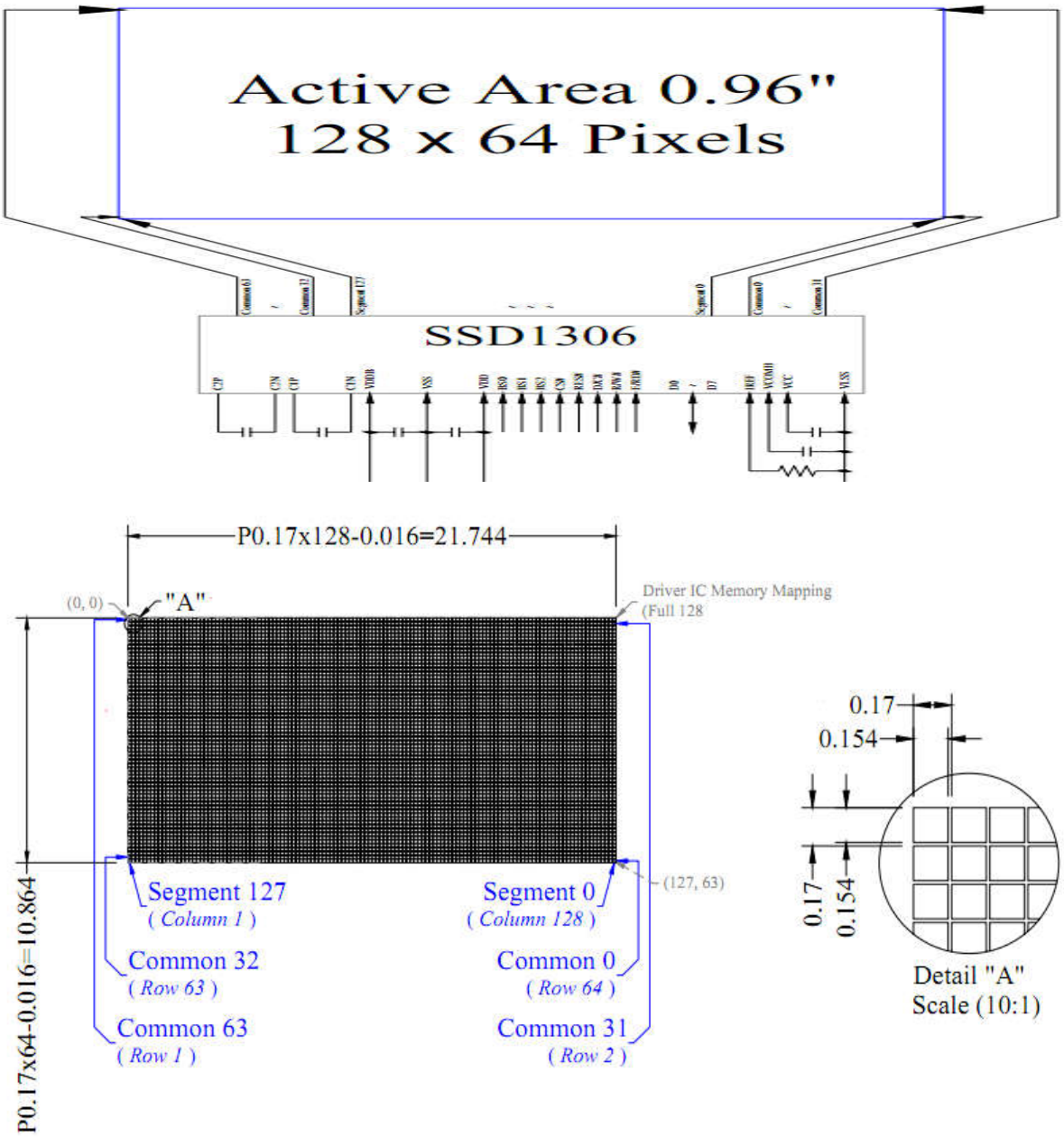
2. MECHANICAL SPECIFICATIONS

ITEM	SPECIFICATIONS	UNIT
Module Size	27.5L×27.8W×3.0(MAX)H	mm
View Area	23.74×13.204	mm
Effective Area	21.74×11.204	dots
Pixel Size	0.15×0.15	mm
Pixel Pitch	0.17×0.17	mm

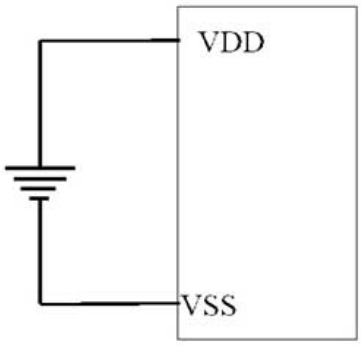
3. EXTERNAL DIMENSIONS



4. BLOCK DIAGRAM



5. POWER SUPPLY



6. PIN DESCRIPTION

ITEM	SYMBOL	LEVEL	FUNCTION
1	VSS	0V	Power Ground
2	VDD	+3.3V~5.0V	Power Supply For Logic
3	SCL	H/L	Serial Clock signal
4	SDA	H/L	Serial Data input signal

7 . Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	Vdd	-0.3	4	V	1, 2
Supply Voltage for Display	Vcc	0	11	V	1, 2
Supply Voltage for DC/DC	VDDB	-0.3	5	V	1, 2
Operating Temperature	Top	-40	70	℃	-
Storage Temperature	Tst	-40	85	℃	-
Life Time (120 cd/mm)		10,000	-	hour	4
Life Time (80 cd/mm)		30,000	-	hour	4
Life Time (60 cd/mm)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80° C.

Note 4: V_{CC} = 9.0V, T_a = 25°C, 50% Checkerboard.

Software configuration follows Section 4.4 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

8 . ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	TYP	Max	Unit
Supply Voltage for Logic	VDD		3.0	3.3	5.0	V
Supply Voltage for Display (Supplied Externally)	VCC	Note 5 (Internal DC/DC Disable)	8.5	9.0	9.5	V
Supply Voltage for DC/DC	VDDB	Internal DC/DC Enable	3.5	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	VCC	Note 6 (Internal DC/DC Enable)	7.0	-	7.5	V
High Level Input	VIH	IOUT = 100μA, 3.3MHz	0.8×V	-	VDD	V

			DD			
Low Level Input	VIL	IOUT = 100μA, 3.3MHz	0	-	0.2×VDD	V
High Level Output	VOH	IOUT = 100μA, 3.3MHz	0.9×VDD	-	VDD	V
Low Level Output	VOL	IOUT = 100μA, 3.3MHz	0	-	0.1×VDD	V
Operating Current for VDD	IDD		-	180	300	μA
Operating Current for VCC (VCC Supplied Externally)	ICC	Note 7	-	5.1	6.4	mA
		Note 8	-	7.3	9.1	mA
		Note 9	-	12.3	15.4	mA
Operating Current for VDDB (VCC Generated by Internal DC/DC)	IDDB	Note 10	-	13.0	16.3	mA
		Note 11	-	18.8	23.5	mA
		Note 12	-	25.6	32.0	mA
Sleep Mode Current for VDD	IDD, SLEEP		-	1	5	μA
Sleep Mode Current for VCC	ICC, SLEEP		-	2	10	μA

Note 5 & 6: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer's request.

Note 7: VDD = 2.8V, VCC = 9.0V, 30% Display Area Turn on.

Note 8: VDD = 2.8V, VCC = 9.0V, 50% Display Area Turn on.

Note 9: VDD = 2.8V, VCC = 9.0V, 100% Display Area Turn on.

Note 10: VDD = 2.8V, VCC = 7.25V, 30% Display Area Turn on.

Note 11: VDD = 2.8V, VCC = 7.25V, 50% Display Area Turn on.

Note 12: VDD = 2.8V, VCC = 7.25V, 100% Display Area Turn on.

9 . Optical Characteristics

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Brightness (VCC Supplied Externally)	Lbr	Note 5	100	120	-	cd/mm
Brightness (VCC Generated by Internal DC/DC)	Lbr	Note 6	70	90	-	cd/mm
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at VDD = 2.8V, VCC = 9V & 7.25V.
Software configuration follows Section 4.4 Initialization.

10. COMMAND TABLE

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0 0 0 0 0	26/27 A[7:0] B[2:0] C[2:0] D[2:0] E[7:0] F[7:0]	0 0 * * * 0 1	0 0 * * * 0 1	1 0 * * * 0 1	0 0 * * * 0 1	0 0 * * * 0 1	1 0 B_2 C_2 D_2 0 1	1 0 B_1 C_1 D_1 0 1	X_0 0 B_0 C_0 D_0 0 1	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames | 100b – 3 frames 001b – 64 frames | 101b – 4 frames 010b – 128 frames | 110b – 25 frame 011b – 256 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Dummy byte (Set as FFh)
0 0 0 0 0 0	29/2A A[2:0] B[2:0] C[2:0] D[2:0] E[5:0]	0 0 * * * *	0 0 * * * *	1 0 * * * E_5	0 0 * * * E_4	1 0 * * * E_3	0 0 B_2 C_2 D_2 E_2	X_1 0 B_1 C_1 D_1 E_1	X_0 0 B_0 C_0 D_0 E_0	Continuous Vertical and Horizontal Scroll Setup	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames | 100b – 3 frames 001b – 64 frames | 101b – 4 frames 010b – 128 frames | 110b – 25 frame 011b – 256 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows **Note** (1) No continuous vertical scrolling is available.

2. Scrolling Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode

3. **Addressing Setting Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode

4. **Hardware Configuration (Panel resolution & layout related) Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.

4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0 0	DB A[6:4]	1 0	1 A_6	0 A_5	1 A_4	1 0	0 0	1 0	1 0	Set V_{COMH} Deselect Level	A[6:4] / Hex code / V_{COMH} deselect level 000b / 00h / ~ 0.65 x V_{CC} 010b / 20h / ~ 0.77 x V_{CC} (RESET) 011b / 30h / ~ 0.83 x V_{CC}
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

6. Advance Graphic Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	23 A[6:0]	0 *	0 *	1 A5	0 A4	0 A3	0 A2	1 A1	1 A0	Set Fade Out and Blinking	A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET] A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Blinking mode. Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and than contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled. A[3:0] : Set time interval for each fade step A[3:0] | Time interval for each fade step 0000b | 8 Frames 0001b | 16 Frames 0010b | 24 Frames : | : 1111b | 128 Frames Note (1) Refer to section 10.3.1 for details.
0 0	D6 A[0]	1 0	1 0	0 0	1 0	0 0	1 0	1 0	0 A0	Set Zoom In	A[0] = 0b Disable Zoom in Mode[RESET] A[0] = 1b Enable Zoom in Mode Note (1) The panel must be in alternative COM pin configuration (command DAh A[4] =1) (2) Refer to section 10.3.2 for details.

7. Charge Pump Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	8D A[7:0]	1 *	0 *	0 0	0 1	1 0	1 A_2	0 0	1 0	Charge Pump Setting	A[2] = 0b, Disable charge pump(RESET) A[2] = 1b, Enable charge pump during display on **Note** (1) The Charge Pump must be enabled by the following command sequence: 8Dh ; Charge Pump Setting 14h ; Enable Charge Pump AFh; Display ON

Note
(1) "*" stands for "Don't care".

For detailed instruction information, see SSD1306 datasheet .

11 . MPU Interface

Conditions:

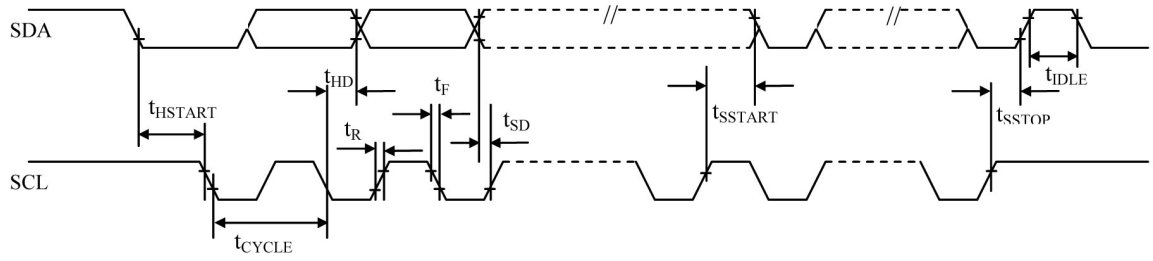
V_{DD} - V_{SS} = V_{DD} - V_{SS} = 1.65V to 3.3V

T_A = 25°C

Table 13-6 :I^2C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 13-5 : I^2C interface Timing characteristics



MCU I2C Interface

The I2C communication interface consists of slave address bit SA0, I2C-bus data signal SDA (SDAOUT/D2 for
output and SDAIN/D1 for input) and I2C-bus clock signal SCL (D0). Both the data and clock signals must be
connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)

SSD1306 has to recognize the slave address before transmitting or receiving any information by the I2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b7 b6 b5 b4 b3 b2 b1 b0

0 1 1 1 1 0 SA0 R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, can be selected as the slave address of SSD1306. D/C# pin acts as SA0 for slave address selection.

“R/W#” bit is used to determine the operation mode of the I2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I2C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.

“SDAIN” and “SDAOUT” are tied together and serve as SDA. The “SDAIN” pin must be connected to act as SDA. The “SDAOUT” pin may be disconnected. When “SDAOUT” pin is disconnected, the acknowledgement signal will be ignored in the I2C-bus.

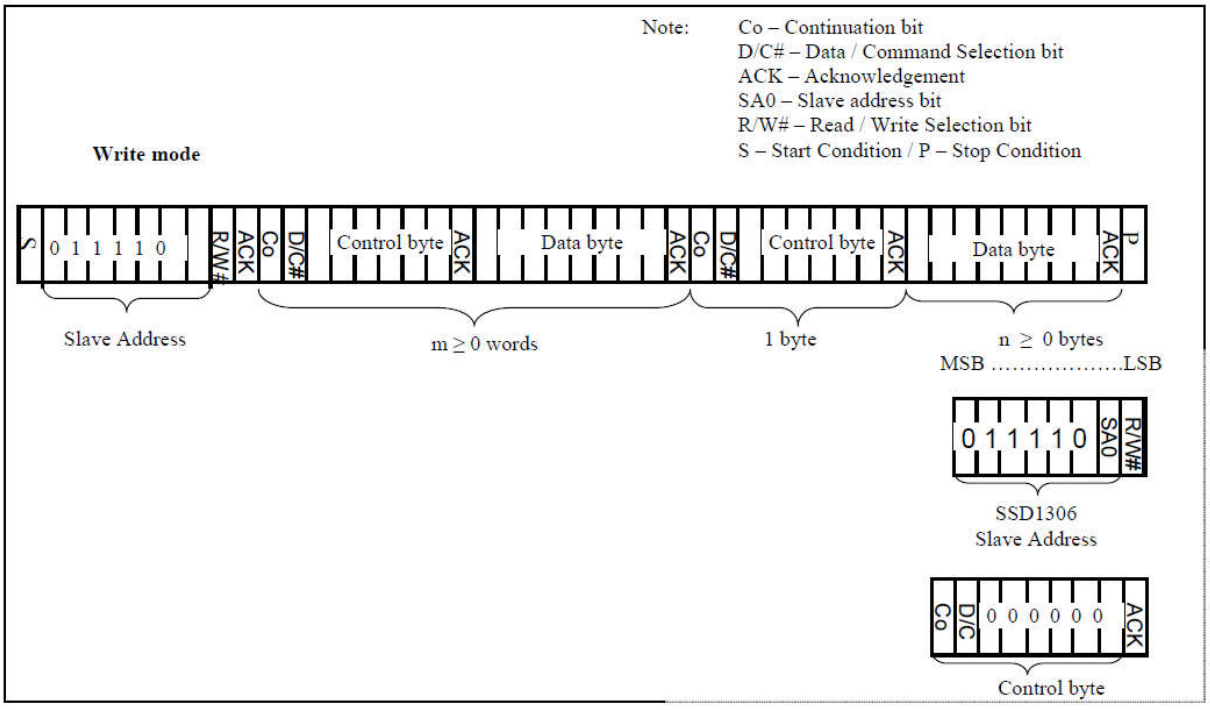
c) I2C-bus clock signal (SCL)

The transmission of information in the I2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

I2C-bus Write data

The I2C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I2C-bus in chronological order.

Figure 8-7 : I²C-bus data format



Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.

2) The slave address is following the start condition for recognition use. For the SSD1306, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 8-8 : Definition of the Start and Stop Condition

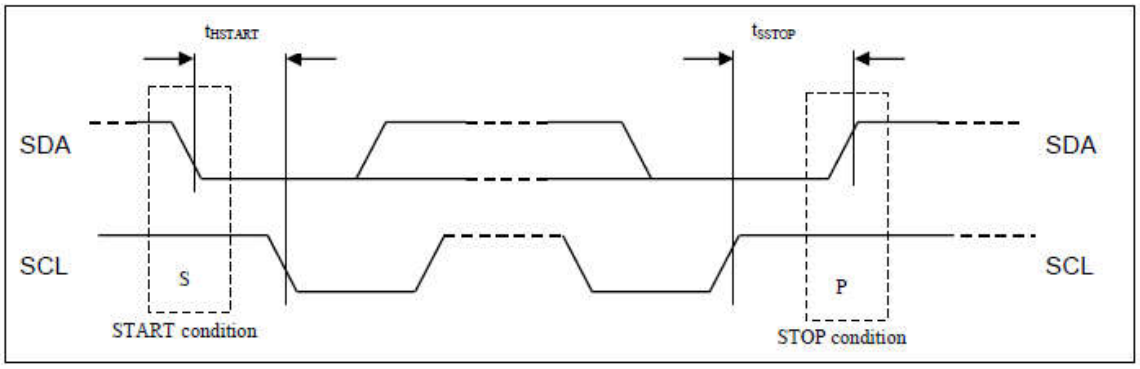
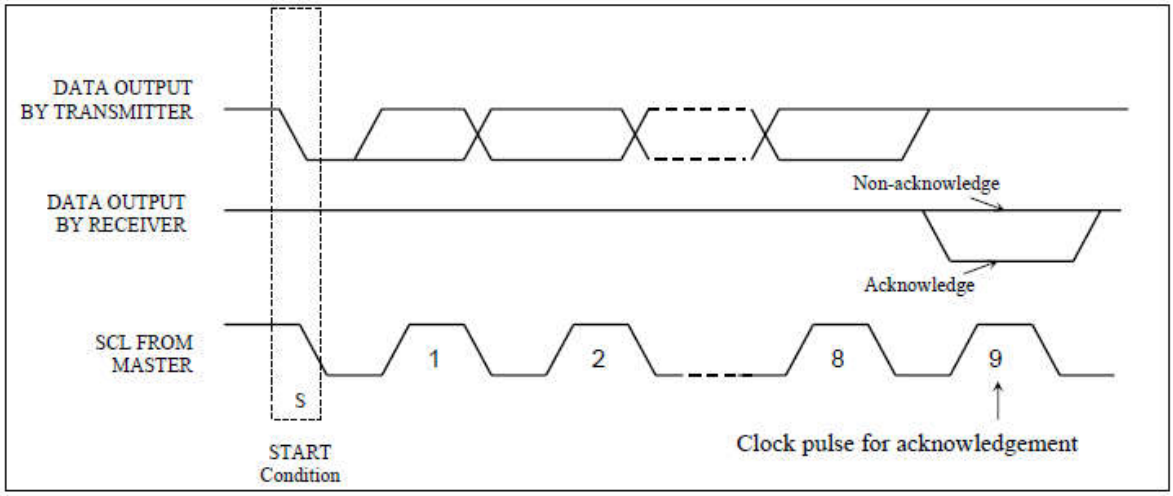


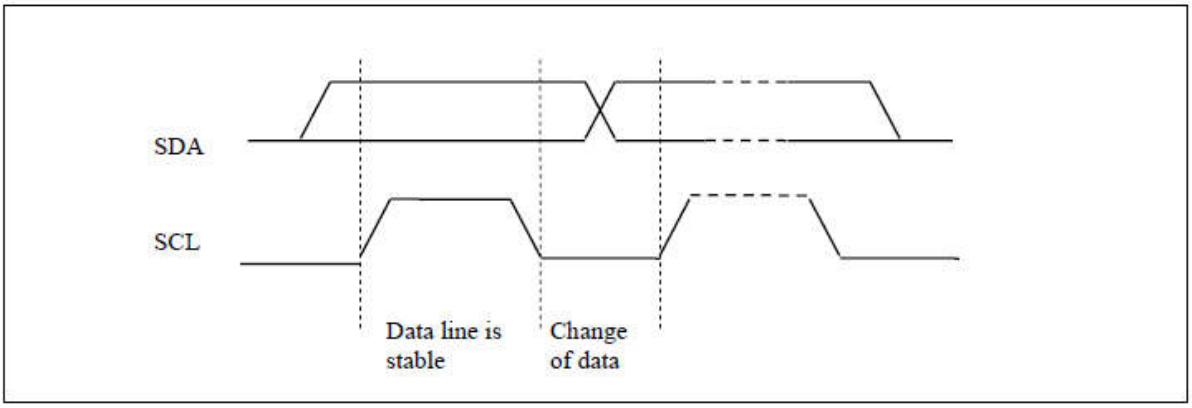
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

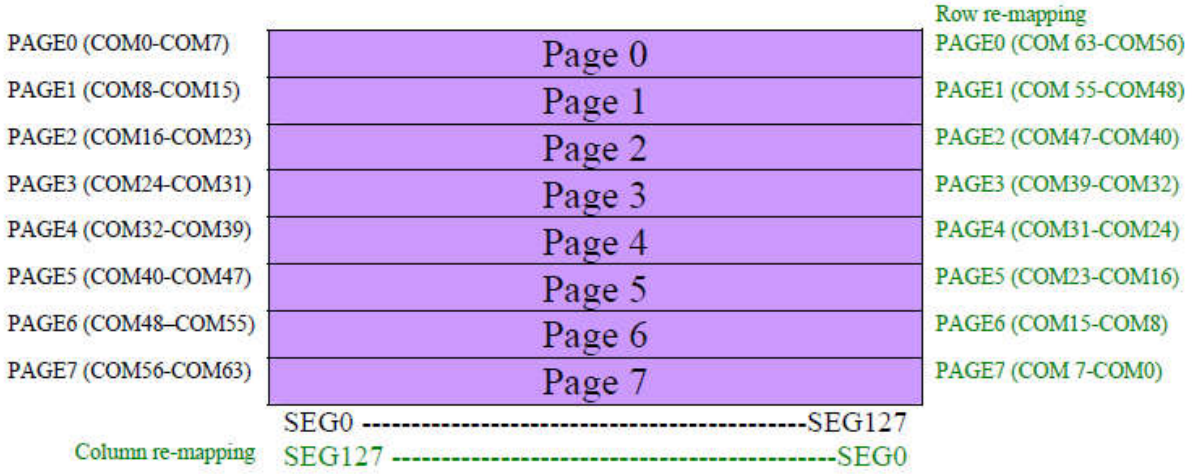
Figure 8-10 : Definition of the data transfer condition



12. Graphic Display Data RAM (GDDRAM)

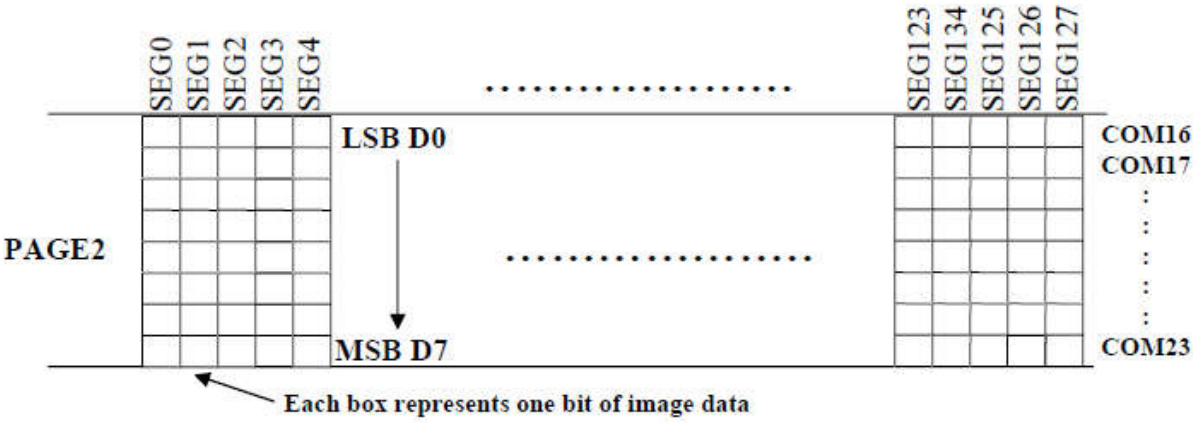
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is
128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Figure 8-13 : GDDRAM pages structure of SSD1306



When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.
For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

13. Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF

2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

14 . DESIGN AND HANDING PRECAUTION

14.1 The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.

14.2 The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

14.3 Never attempt to disassemble or rework the LCD module.
14.4 Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
14.5 When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
14.6 Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result
14.7 Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
14.8 Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
14.9 LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
14.10 When peeling of the protective film form LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
14.11 Take care and prevent get hurt by the LCD panel edge.
14.12 Never operate the LCD module exceed the absolute maximum ratings.
14.13 Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
14.14 Never apply signal to the LCD module without power supply.
14.15 IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
14.16 LCD module reliability may be reduced by temperature shock.
14.17 When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module